International Journal of Electrical and Electronics Research ISSN 2348-6988 (online)
Vol. 3, Issue 1, pp: (80-84), Month: January - March 2015, Available at: www.researchpublish.com

Reduction in Total Harmonic Distortion Using Multilevel Inverters

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Abstract: **The main concept of a multilevel converter is to achieve higher power by using a series of power semiconductor switches with several dc source to perform the power conversion by synthesizing a staircase voltage waveform. In this paper, 3- level and 5- level diode clamped inverter topologies and SPWM technique has been applied to formulate the switching pattern for inverter that minimize the harmonic distortion at the output.**

***Keywords*:** **Diode Clamped Inverter, Total Harmonic Distortion, SPWM.**

I. INTRODUCTION

Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveform having large number of steps. It include an array of power semiconductors and dc voltage sources, the output of which generate voltages with stepped waveforms .The steps being supplied from different DC levels supported by

series connected batteries or capacitors[1]. The unique structure of multi- level inverter allows them to reach high voltages and therefore lower voltage rating device can be used. As the number of levels increases, the synthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. Among various modulation techniques [2] for a multilevel inverter, sin-triangle pulse width modulation (SPWM) is an attractive technique due to the following merits. It proportionally varies the width of each pulse to the amplitude of a sine wave evaluated at the center of the same pulse. It is suitable for MATLAB/SIMULINK implementation. .As number of levels of diode clamped inverter increases then there is reduction of total harmonics distortion (THD) of inverter output voltage. This is the main advantage of the proposed control method

MULTILEVEL INVERTER TOPOLOGIES:

The basic three types of multilevel topologies used are: (1) Diode clamped multilevel inverters (2) Flying capacitors multilevel inverter or capacitor clamped multilevel inverter (3) Cascaded inverter with separate DC sources.[3].

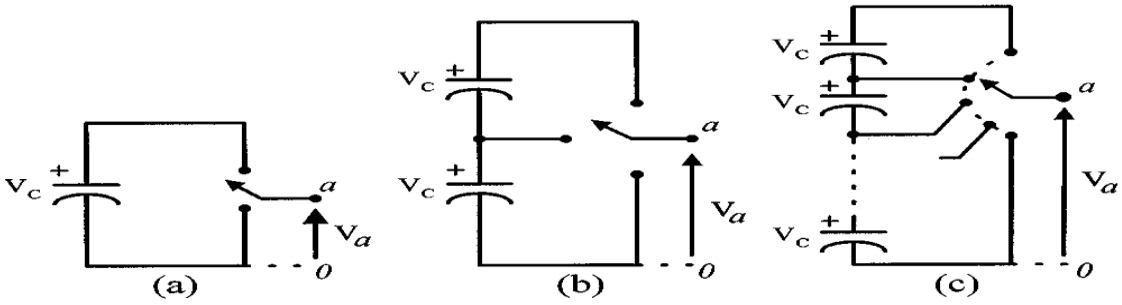

Fig.1.One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n level

A preferred multilevel inverter topology shall have the following Characteristics(1)The level is easy to extend (2)When the number of levels is high enough, the harmonic content is low(3)There is no need for filters (4)Inverter efficiency is high because all devices are switched at the fundamental frequency(5)The control method is simple. Fig (1) shows a schematic diagram of one phase leg of inverters with different number of levels for which the action of the power semiconductors is represented by an ideal switch with several positions.

II. INVERTER TOPOLOGY

***Neutral Point-Clamped Inverter*:**

The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter [4] .In general for an N level diode clamped inverter, for each leg, 2(N-1) switching devices, (N-1)*(N-2) clamping diodes and (N-1) dc link capacitors are required. By increasing the number of voltage levels the quality of the output voltage is improved and the voltage waveform becomes closer to sinusoidal waveform. However, capacitor voltage balancing will be the critical issue in high level inverters. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement.[5]

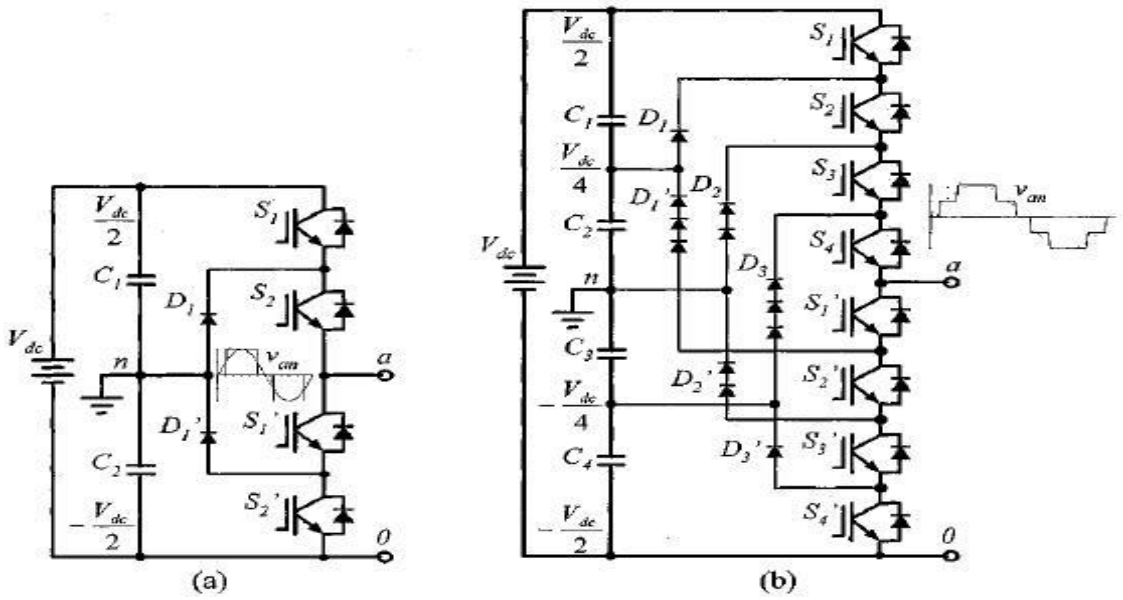

Fig. 2. Diode-clamped multilevel inverter circuit topologies. (a)Three-level. (b) Five-level

A three-level and five-level diode clamped inverter are shown in Fig.2(a)and Fig.2(b) respectively For a three- level inverter , a set of two switches is on at any given time and in five-level inverter, a set of four switches is on at any given time and so on .Switching states in one leg of three-level and five-level diode clamped inverter and are shown in Table-I and Table-II.

TABLE-I SWITCHING STATES FOR THREE LEVEL INVERTER

SWITCH STATUS	STATE	POLE VOLTAGE
S_1=ON,S_2=ON,S_1'=OFF,S_2'=OFF	S=+ve	$V_{ao}=V_{dc}/2$
S_1=OFF,S_2=ON,S_1'=ON,S_2'=OFF	S=0	$V_{ao}=0$
S_1=OFF,S_2=OFF,S_1'=ON,S_2'=ON	S=-ve	$V_{ao}=-V_{dc}/2$

TABLE-II SWITCHING STATES FOR FIVE LEVEL INVERTER

VOLTAGE Vao	SWITCH STATES							
	S1	S2	S3	S4	S1'	S2'	S3'	S4'
$V_{ao}=V_{dc}$	1	1	1	1	0	0	0	0
$V_{ao}=V_{dc}/2$	0	1	1	1	1	0	0	0
$V_{ao}=0$	0	0	1	1	1	1	0	0
$V_{ao}=-V_{dc}/2$	0	0	0	1	1	1	1	0
$V_{ao}=-V_{dc}$	0	0	0	0	1	1	1	1

III. SPWM (SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE)

Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers [6].THD of phase-shifted modulation is much higher than level-shifted modulation. An m-level inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are continuous. The pulse generator is modeled where one reference wave (sine wave) and two carrier waves (triangular wave) are superimposed. Based on the modulation techniques, pulses are generated by comparing modulating signal with carrier signal. These pulses are added in order to get an aggregated signal. Pulses which are to be given to the switches in one phase leg of a three level inverter are derived from an aggregated signal. Similarly the pulses are generated for remaining two phases, just by changing phase shifting angle of modulating signal by 120 degrees.[7] Five level inverter is modeled in the same way as the three level inverter. The difference here is the number of carrier signal.

Inverter output voltage, $V_{AO}=V_{dc}/2$, When $V_{control}>V_{tri,}$ and $V_{AO}=-V_{dc}/2$, When $V_{control}<V_{tri}$. PWM frequency is the same as the frequency of V_{tri}. Amplitude is controlled by the peak value of $V_{control}$ and Fundamental frequency is controlled by the frequency of $V_{control}$. Modulation Index (m) is given by: [8]

$$m=\frac{Vcontrol}{Vtri}=\frac{peak\ of\ (VAO)1}{Vdc/2}$$, Where $(V_{AO})_1$ is the fundamental frequency component of V_{AO}

IV. SIMULATION

The fig (3) shows the MATLAB/SIMULINK MODEL for 3-level neutral clamped multilevel inverter with PWM technique. The fig.(4) shows the Matlab/Simulink model of three phase 5-Level neutral clamped multilevel inverter.

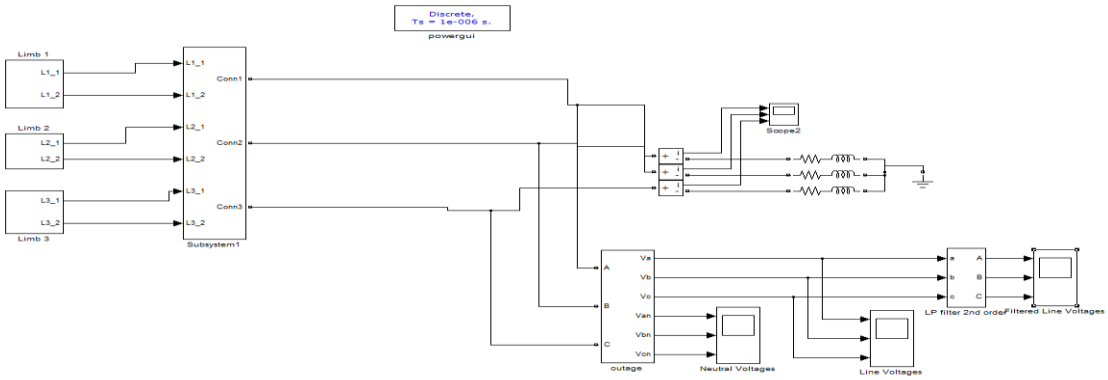

Fig.3.Simulation circuit of Three-Level diode-clamped inverter

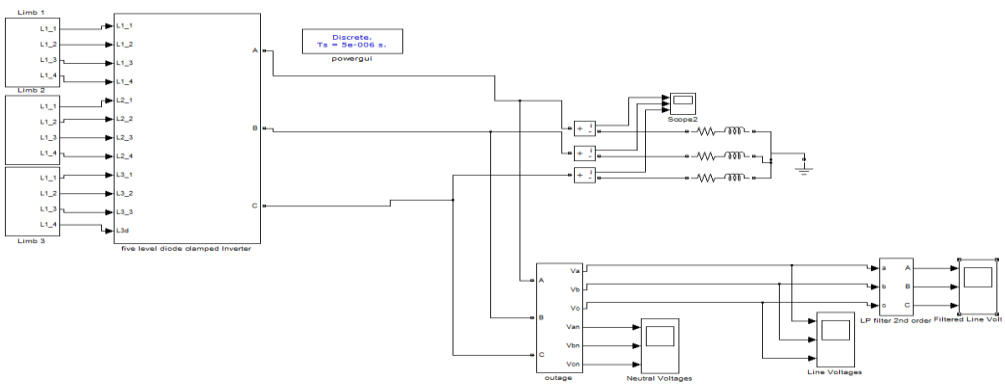

Fig 4.Simulation circuit of Five-Level diode-clamped inverter

V. SIMULATION RESULTS

To verify the proposed scheme, MATLAB/SIMULINK software is used. Simulation results show that as inverter level increases from 3-level to 5-level total harmonic distortion reduces to 17.37% from 43.63%. Line voltage waveform for RL load for three-level inverter, Line voltage waveform for RL load for Five - level inverter and comparison of THD of three-level and five level diode clamped inverter has been shown in fig (5) and fig (6).

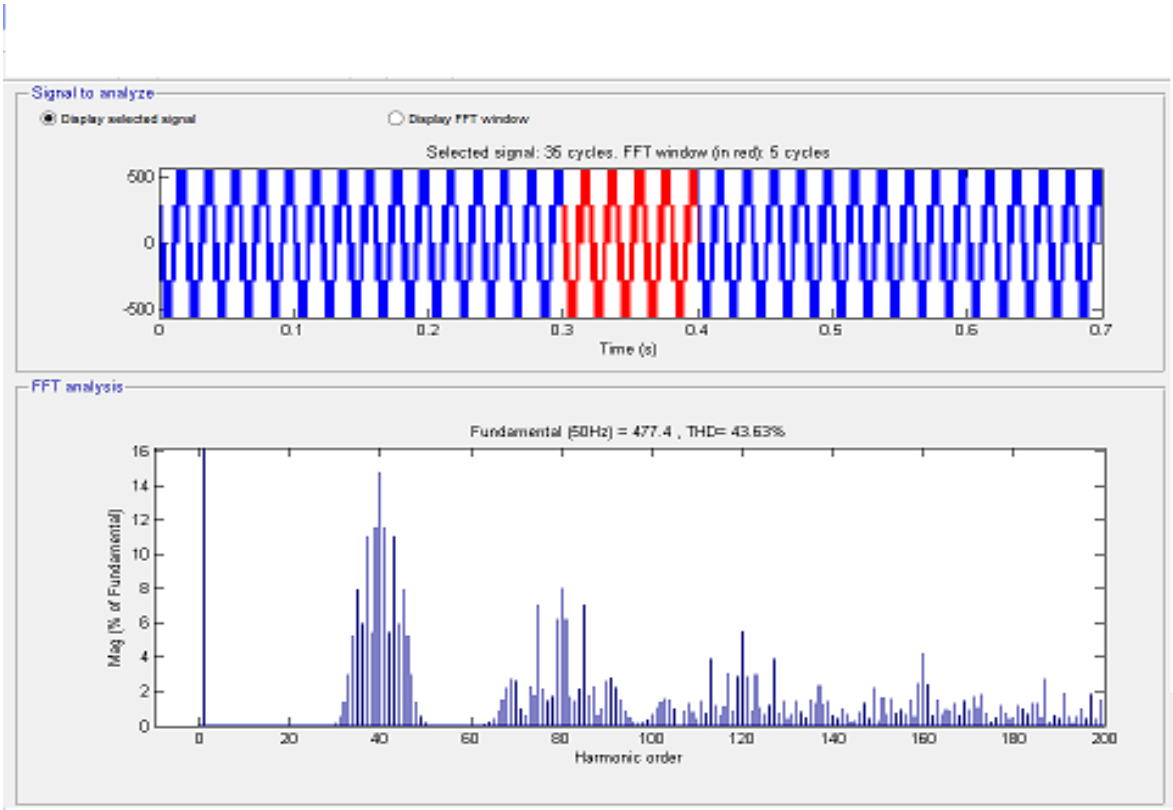

Fig.5. Line Voltage and Harmonic Spectrum of 3-level Diode clamped multilevel inverter

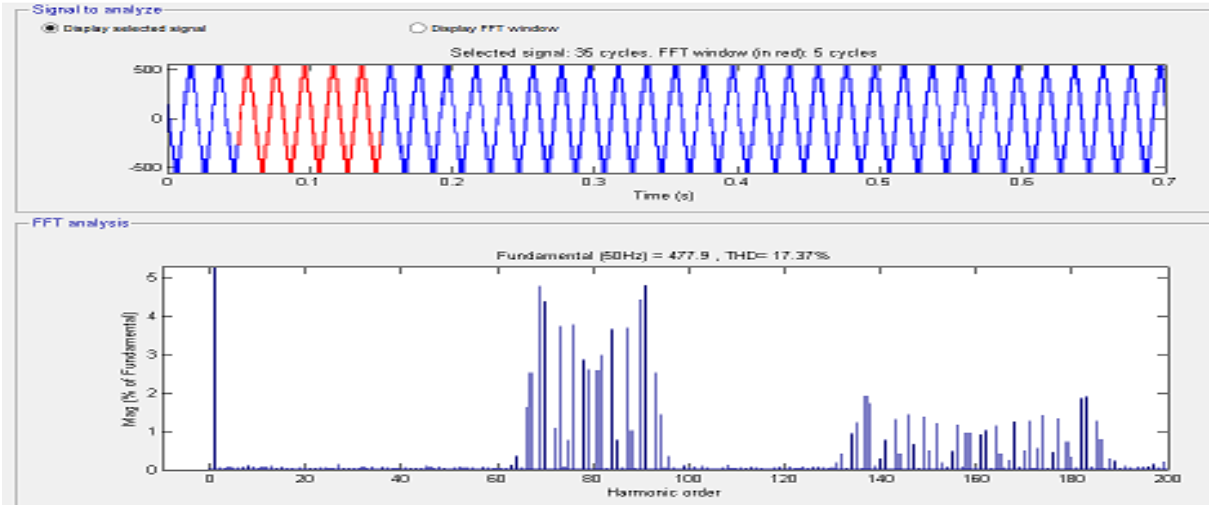

Fig.6. Line Voltage and Harmonic Spectrum of 5-level Diode clamped multilevel inverter .

The proposed inverter scheme was simulated using Simulink /matlab 2009. Parameters used for simulation are as follows: fm = 50Hz, fc= 10 kHz. . DC voltage of the inverter for three level is V_{dc}=*282.5V*and for five level V_{dc}=*141.2V*. Load is assumed to be of RL load where R=15 Ohms, L=24.2 mH. The total harmonic distortion analysis has been done for voltages and currents of three level and five level inverter and their values are compared and shown in Table-III.

TABLE-III REDUCTION OF THD BY VARYING INVERTER LEVEL

Parameters (line voltages and phase currents)	3-level (% THD values)	5-level (% THD values)
V_{ab}	*43.63*	*17.37*
V_{bc}	*43.65*	*17.37*
V_{ca}	*35.32*	*17.32*
I_a	*1.74*	*0.41*
I_b	*1.99*	*0.41*
I_c	*1.74*	*0.41*

VI. CONCLUSION

In this paper SPWM technique is proposed for three-level and five-level Diode clamped inverter. The comparative THD analysis of a three phase 3-level and 5-level neutral clamped multilevel inverter is presented in this paper. SPWM techniques are applied to the three-level and five-level diode clamped inverter. The main feature of the modulation scheme lies in its ability to eliminate the harmonics in inverter output voltage and output current. The lower order harmonics were considerably reduced in the SPWM technique. By increasing the number of levels, the THD will be decreased but on the other hand cost and weight will be increased as well. Also since the switching angles for switches are not the same, the drive circuit for each switch is separate from other switches.

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